Inventor: Arup Bhattacharyya

Title: Semiconductor-On-Insulator Thin Film Transistor Constructions

Assignee: Micron Technology, Inc.

EV317136323

INFORMATION DISCLOSURE STATEMENT

PURSUANT TO 37 C.F.R. §§1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional of co-pending application Serial No. 10/243,180 filed September 12, 2002. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: JULY 22, 2003 Attorney: _____

David G. Latwesen, Ph.D. Reg. #38,533
WELLS ST. JOHN P.S.

EV317136323

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. M122-2362	PRIORITY SERIAL NO 10/243,180
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Arup Bhattacharyya	
		PRIORITY FILING DATE September 12, 2002	PRIORITY GROUP 2818

			OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)
	AA		Ono, K. et al., "Analysis of Current-Voltage Characteristics in Polysilicon TFTs for LCDs", IEDM Tech. Digest, 1988, pp. 256-259.
	AB		Yamauchi, N. et al., "Drastically Improved Performance in Poly-Si TFTs with Channel Dimensions Comparable to Grain Size", IEDM Tech. Digest, 1989, pp. 353-356.
	AC		King, T. et al, "A Low-Temperature (≤550°C) Silicon-Germanium MOS Thin-Film Transistor Technology for Large-Area Electronics", IEDM Tech. Digest, 1991, pp. 567-570.
	AD		Kuriyama, H. et al., "High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics", IEDM Tech. Digest, 1991, pp. 563-566.
	AE		Jeon, J. et al., "A New Poly-Si TFT with Selectively Doped Channel Fabricated by Novel Excimer Laser Annealing", IEDM Tech. Digest, 2000, pp. 213-216.
	AF		Kim, C.H. et al., "A New High -Performance Poly-Si TFT by Simple Excimer Laser Annealing on Selectively Floating a-Si Layer", IEDM Tech. Digest, 2001, pp. 751-754.
	AG		Hara, A. et al, "Selective Single-Crystalline-Silicon Growth at the Pre-Defined Active Regions of TFTs on a Glass by a Scanning CW Layer Irradiation", IEDM Tech. Digest, 2000, pp. 209-212.
	AH		Hara, A. et al., "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization", IEDM Tech. Digest, 2001, pp. 747-750.
	AI		Jagar, S. et al., "Single Grain Thin-Fim-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization", IEDM Tech. Digest, 1999, p. 293-296.
	AJ		Gu, J. et al., "High Performance Sub-100 nm Si Thin-Film Transistors by Pattern-Controlled Crystallization of Thin Channel Layer and High Temperature Annealing", DRC Conference Digest, 2002, pp. 49-50.
	AK		Kesan, V. et al., "High Performance 0.25μm p-MOSFETs with Silicon- Germanium Channels for 300K and 77K Operation", IEDM Tech. Digest, 1991, pp. 25-28.
	AL		Garone, P.M. et al., "Mobility Enhancement and Quantum Mechanical Modeling in Ge_xSi_{1-x} Channel MOSFETs from 90 to 300K", IEDM Tech. Digest, 1991, pp. 29-32.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EV331736823

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2362	PRIORITY SERIAL NO 10/243,180
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Arup Bhattacharyya	
		PRIORITY FILING DATE September 12, 2002	PRIORITY GROUP 2818

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
	AM		Feder, B.J., "I.B.M. Finds Way to Speed Up Chips", The New York Times, June 8, 2001, reprinted from http://www.nytimes.com/2001/06/08 /technology/08BLUE.html, 2 pgs.
	AN		Rim, K. et al., "Strained Si NMOSFET's for High Performance CMOS Technology", 2001 Sympos. on VLSI Tech. Digest of Technical Papers, p. 59-60.
	AO		Li, P. et al., "Design of High Speed Si/SiGe Heterojunction Complementary MOSFETs with Reduced Short-Channel Effects", Natl. Central University, ChungLi, Taiwan, ROC, Aug. 2001, Contract No. NSC 89-2215-E-008-049, National Science Council of Taiwan., pp. 1, 9.
	AP		Ernst, T. et al., "Fabrication of a Novel Strained SiGe:C-channel Planar 55 nm nMOSFET for High-Performance CMOS", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 92-93.
	AQ		Rim, K. et al., "Characteristics and Device Design of Sub-100 nm Strained SiN- and PMOSFETs", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 98-99.
	AR		Belford, R.E. et al., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", DRC Conf. Digest, 2002, pp. 41-42.
	AS		Shima, M. et al., "<100> Channel Strained-SiGe p-MOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 94-95.
	AT		Nayfeh, H.M. et al., "Electron Inversion Layer Mobility in Strained-Si n-MOSFET's with High Channel Doping Concentration Achieved by Ion Implantation", DRC Conf. Digest, 2002, pp. 43-44.
	AU		Bae, G.J. et al., "A Novel SiGe-Inserted SOI Structure for High Performance PDSOI CMOSFET", IEDM Tech. Digest, 2000, pp. 667-670.
	AV		Cheng, Z. et al., "SiGe-on-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation" and conference outline, MIT Microsystems, Tech. Labs, Cambridge, MA, 2001 IEEE Internatl. SOI Conf., 10/01, pp. 13-14, 3-pg. outline.
	AW		Huang, L.J. et al., "Carrier Mobility Enhancement in Strained Si-on-Insulator Fabricated by Wafer Bonding", 2001 Sympos. on VLSI Tech. Digest of Technical Papers, pp. 57-58.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2362	PRIORITY SERIAL NO 10/243,180
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Arup Bhattacharyya	
		PRIORITY FILING DATE September 12, 2002	PRIORITY GROUP 2818

EV331713623US

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
	AX		Mizuno, T. et al., "High Performance CMOS Operation of Strained-SOI MOSFETs Using Thin Film SiGe-on-Insulator Substrate", 2002 Sympos. on VLSI Tech. Digest of Technical Papers, p. 106-107.
	AY		Tezuka, T. et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique", 2002 VLSI Tech. Digest of Technical Papers, pp. 96-97.
	AZ		Takagi, S., "Strained-Si- and SiGe-on-Insulator (Strained SOI and SGOI) MOSFETs for High Performance/Low Power CMOS Application", DRC Conf. Digest, 2002, pp. 37-40.
	BA		"IBM Builds World's Fastest Communications Microchip", Reuters U.S. Company News, 2/25/2002, reprinted from http://activequote300.fidelity.com/rtrnews/ individual_n.../..., 1 pg.
	BB		Markoff, J., "I.B.M. Circuits are Now Faster and Reduce Use of Power", The New York Times, Feb. 25, 2002, reprinted 3/20/02 from http://story.news.yahoo.com/ news?tmpl=story&u=/nyt/20020225/..., 1 pg.
	BC		Park, J.S. et al., "Normal Incident SiGe/Si Multiple Quantum Well Infrared Detector", IEDM Tech. Digest, 1991, pp. 749-752.
	BD		Current, M.I. et al., "Atomic-Layer Cleaving with Si_xGe_y Strain Layers for Fabrication of Si and Ge-Rich SOI Device Layers", 2001 IEEE Internatl. SOI Conf. 10/01, pp. 11-12.
	BE		Bhattacharyya, A., "The Role of Microelectronic Integration in Environmental Control: A Perspective", Mat. Res. Soc. Symp. Proc. Vol. 344, 1994, pp. 281-293.
	BF		Myers, S.M. et al., "Deuterium Interactions in Oxygen-Implanted Copper", J. Appl. Phys., Vol. 65(1), Jan. 1, 1989, p. 311-321.
	BG		Saggio, M. et al., "Innovative Localized Lifetime Control in High-Speed IGBT's", IEEE Elec. Dev. Lett., V. 18, No. 7, July 1997, pp. 333-335.
	BH		Lu, N.C.C. et al., "A Buried-Trench DRAM Cell Using a Self-Aligned Epitaxy Over Trench Technology", IEDM Tech. Digest, 1988, pp. 588-591.
	BI		Yamada, T. et al., "Spread Source/Drain (SSD) MOSFET Using Selective Silicon Growth for 64Mbit DRAMs", IEDM Tech. Digest, 1989, pp. 35-38.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2362	PRIORITY SERIAL NO 10/243,180
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Arup Bhattacharyya	
		PRIORITY FILING DATE September 12, 2002	PRIORITY GROUP 2818

			OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)
	BJ		van Meer, H. et al., "Ultra-Thin Film Fully-Depleted SOI CMOS with Raised G/S/D Device Architecture for Sub-100
			nm Applications", 2001 IEEE Internatl. SOI Conf. 10/01, pp. 45-46.
	BK		
	BL		
	BM		
	BN		
	BO		
	BP		
	BQ		
	BR		
	BS		
	BT		

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EV317136323